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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/614,001	07/08/2003	Shibly S. Ahmed	H1484	6254

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EXAMINER	
FENTY, JESSE A	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 09/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/614,001	AHMED ET AL.
	Examiner	Art Unit
	Jesse A. Fenty	2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,14-19 and 21-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,14-19 and 21-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/23/03,07/14/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. Claims 1-7, 14-18 and 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fried et al. (U.S. Patent No. 6,657,259 B2) in view of Wang et al. (U.S. Patent No. 6,589,836 B1) and further in view of Dash et al. (U.S. Patent No. 4,399,605) and Moslehi (U.S. Patent No. 5,397,909).

In re claim 1, Fried (Fig. 7b) discloses a semiconductor device, comprising:

A substrate (202);

An insulating layer (204) formed on the substrate;

A first device formed on the insulating layer, including:

A first fin (206) formed on the insulating layer, and

A first silicided gate (212; column 10, lines 7-8) formed over a portion of the first fin and including a first thickness of silicide material; and

A second device formed on the insulating layerr, including:

A second fin (206) formed on the insulating layer, and

A second silicided gate (212) formed over a portion of the second fin and including a second thickness of silicide material.

Fried discloses a layer of silicide (212) atop the gate regions but does not expressly disclose the silicide regions over each gate region comprising a separate silicide thickness. Wang (Fig. 7) discloses thin (15b) and thick (15c) silicide layers atop gate structures (6). It would have been obvious for one skilled in the art at the time of the invention to use replace the

uniform thickness silicide layers of Fried with the dual thickness silicide layers disclosed by Wang for the purpose, for example, of diversifying the device by varying the resistance of the gate layers (Wang; column 4, lines 54-57), wherein

A threshold voltage of the second device varies about 200 millivolts to about 400 millivolts from a threshold voltage of the first device.[1]

In re claim 2, Fried in view of Wang discloses the device of claim 1, further comprising:

A first dielectric layer (Fried, 208; column 8, lines 1-6) formed between the first fin and the first silicide gate and wherein the second device further includes:

A second dielectric layer (Fried, 208) formed between the second fin and the second silicided gate.

In re claim 3, Fried in view of Wang discloses the device of claim 1, wherein the first silicide gate is partially silicided and the first thickness ranges from about 100 to 500 angstroms (Wang; column 4, lines 60-63).

In re claim 4, Fried in view of Wang discloses the device of claim 1, wherein the second silicided gate is fully silicided.

In re claim 5, Fried in view of Wang discloses the device of claim 4, wherein the second thickness ranges from about 400 to 1000 angstroms (Wang; column 4, lines 50-54).

In re claim 6, Fried in view of Wang discloses the device of claim 1, wherein the first device is a NMOS device and the second device is a PMOS device (Fried, column 8, lines 1-30; Wang; column 4, lines 50-63).

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[1] The effects of silicide on threshold voltage is known in the art as disclosed by Dash et al. (U.S. Patent No. 4,399,6054) in column 4, lines 41-46 and Lund et al. (U.S. Patent No. 4,319,395) in columns 5-6, lines 65-68 and 1-2. Though empirical values are not given, the claimed values are an inherent characteristic of the material and do

In re claim 7, Fried (Fig. 8) in view of Wang discloses the device of claim 1, wherein the first device and the second device are included in a single circuit element (Fried; column 11, lines 64-67; column 12, lines 1-8).

In re claim 14, Fried (Fig. 7b) discloses a semiconductor device, comprising:

A substrate (202);

An insulating layer (204) formed on the substrate;

A first device formed on the insulating layer, including:

A first fin (206) formed on the insulating layer,

A first dielectric layer (208; column 8, lines 1-6) formed on the first fin, and

A silicided gate (212) formed over a portion of the first find and the first dielectric layer; and

A second device formed on the insulating layer, including:

A second fin (206) formed on the insulating layer,

A second dielectric layer (208) formed on the second fin, and

A silicided gate (212) formed over a portion of the second fin and the second dielectric layer, wherein

A threshold voltage of the second device varies about 200 millivolts to about 400 millivolts from a threshold voltage of the first device.[2]

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not represent values that could not have been obtained through routine experimentation. Therefore, the cited art is adequate to reject the claim.

[2] The effects of silicide on threshold voltage is known in the art as disclosed by Dash et al. (U.S. Patent No. 4,399,6054) in column 4, lines 41-46 and Lund et al. (U.S. Patent No. 4,319,395) in columns 5-6, lines 65-68 and 1-2. Though empirical values are not given, the claimed values are an inherent characteristic of the material and do

Fried discloses a layer of silicide (212) atop the gate regions but does not expressly disclose the silicide regions over each gate region comprising a separate silicide thickness. Wang (Fig. 7) discloses thin (15b) and thick (15c) silicide layers atop gate structures (6). It would have been obvious for one skilled in the art at the time of the invention to use replace the uniform thickness silicide layers of Fried with the dual thickness silicide layers disclosed by Wang for the purpose, for example, of diversifying the device by varying the resistance of the gate layers (Wang; column 4, lines 54-57),

In re claim 15, Fried in view of Wang discloses the device of claim 14, wherein the first silicide gate is partially silicided and the first thickness ranges from about 100 to 500 angstroms (Wang; column 4, lines 60-63).

In re claim 16, Fried in view of Wang discloses the device of claim 14, wherein the second thickness ranges from about 400 to 1000 angstroms (Wang; column 4, lines 50-54).

In re claim 17, Fried in view of Wang discloses the device of claim 14, wherein the first device is a NMOS device and the second device is a PMOS device (Fried, column 8, lines 1-30; Wang; column 4, lines 50-63).

In re claim 18, Fried (Fig. 8) in view of Wang discloses the device of claim 14, wherein the first device and the second device are electrically connected (Fried; column 11, lines 64-67; column 12, lines 1-8).

In re claims 21 and 22, Fried in view of Wang discloses the devices of claims 1 and 14 respectively, wherein the width of the fin reaches a lower limit of 200 angstroms (column 7, lines 55-56) but does not expressly disclose the width of the fin being in the range of 10 to 100

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not represent values that could not have been obtained through routine experimentation. Therefore, the cited art is

angstroms. It would have been obvious to one having ordinary skill in the art at the time the invention was made to create a thinner fin since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

In re claim 23, Fried in view of Wang discloses the device of claim 18, wherein a drain of the first fin is electrically connected to a source region of the second fin.[3]

2. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fried in view of Wang as applied to claim14 above, and further in view of Takeda et al. (US 2001/0045589 A1).

In re claim 19, Fried in view of Wang discloses the device of claim 14, but does not expressly disclose a third FET with a third thickness of a silicide region atop the gate. Devices with three FETs overlaid by silicide are well known in the art (Takeda, Fig. 3). It would have been obvious for one skilled in the art at the time of the invention to provide a third FINFET device disclosed in the manner of Fried with a third thickness of silicide as disclosed by Wang for the purpose, for example, of further diversifying the capabilities of the semiconductor device.

Response to Arguments

3. Applicant's arguments filed 06/18/04 have been fully considered but they are not persuasive.

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adequate to reject the claim.

[3] Though Fried shows the two drain regions (306, 312) connected together (Figs. 8, 9), those skilled in the art will recognize that, for the purpose MOSFET fabrication and operation, the appellations source and drain are interchangeable, simply designating the direction of current flowing through the channel. Therefore the connection displayed by Fried of two drain regions connected in series anticipates the claim.

Applicants argue that, neither Fried nor Wang disclose or suggest, either separately, or in combination, the above-mentioned features of amended independent claim 1. For example, Fried and Wang do not disclose or suggest that a threshold voltage of the second device varies about 200 millivolts to about 400 millivolts from a threshold voltage of the first device.

Said argument is addressed in Footnotes 1 and 2 above. Separately, as part of the first office action, as well as the instant rejection, reference is made to Applicant's disclosure as support for the interpretation of the prior art. Applicant admits (in section [0050] of the Specification) that two gate layers with a partially silicided gate and a fully silicided gate, i.e., with different thicknesses, will exhibit different threshold voltages. This teaching is mirrored in the selection of the prior art and provides one of the bases for inherency argued in this rejection.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse A. Fenty whose telephone number is 571-272-1729. The examiner can normally be reached on 5/4-9 1st Fri. Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tom Thomas

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